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Attorney's Docket No. 42P15685
Confirmation No.: 6439

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Scott A. Hareland, et al.

Application No.: 10/607,769

Filed: June 27, 2003

For: Nonplanar Semiconductor Device with
Partially or Fully Wrapped Around Gate
Electrode and Methods of Fabrication

Examiner: Unassigned

Art Unit: 2812

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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If there are any additional charges, please charge Deposit Account No.

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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: February 14, 2006


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Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known

Application Number	10/607,769
Filing Date	June 27, 2003
First Named Inventor:	Scott A. Hareland
Art Unit	2812
Examiner Name	Unassigned
Attorney Docket No.:	42P15685

 Sheet **1** of **2**

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
		US-	2003/0098488 A1	05-29-2003	O'Keeffe et al.	
		US-	2003/0201458 A1	10-30-2003	Clark et al.	
		US-	2004/0262683 A1	12-02-2004	Nihey	
		US-	2004/0180491 A1	09-16-2004	Arai et al.	
		US-	6,635,909 B2	10-21-2003	Clark et al.	
		US-	6,858,478 B2	02-22-2005	Chau et al.	
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FOREIGN PATENT DOCUMENTS

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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/607,769
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				Art Unit	2812
				Examiner Name	Unassigned
Sheet	2	of	2	Attorney Docket Number	42P15685
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
		JING GUO, et al. "Performance Projections for Ballistic Carbon Nanotube Field-Effect Transistors", Applied Physics Letters, Vol. 80, No. 17, pp. 3192-3194 (April 29, 2004)			
		ALI JAVEY, et al., "High-K Dielectrics for Advanced Carbon-Nanotube Transistors and Logic Gates", Advance Online Publication, Published online, pp. 1-6 (November 17, 2002)			
		RICHARD MARTEL, et al., "Carbon Nanotube Field Effect Transistors for Logic Applications" IBM, T.J. Watson Research Center, 2001 IEEE, IEDM 01, pp. 159-162			
		DAVID M. FRIED, et al., "High-Performance P-Type Independent-Gate FinFETs, IEEE Electron Device Letters", Vol 25, No. 4, April 2004, pp. 199-201.			
		DAVID M. FRIED, et al., "Improved Independent Gate N-Type FinFET Fabrication and Characterization", IEEE Electron Device Letters", Vol. 24, No. 9, September 2003, pp. 592-594.			
		CHARLES KUO, et al. "A Capacitorless Double Gate DRAM Technology for Sub-100-nm Embedded and Stand-Alone Memory Applications", IEEE Transactions on Electron Devices", Vol. 50, No. 12, December 2003, pp. 2408-2416.			
		CHARLES KUO, et al., "A Capacitorless Double-Gate DRAM Cell Design for High Density Applications", 2002 IEEE International Electron Devices Meeting Technical Digest, December 2002, pp. 843-846			
		TAKASHI OHSAWA, et al., "Memory Design Using a One-Transistor Gain Cell on SOI", IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp. 1510-1522			
		T. TANAKA, et al., "Scalability Study on a Capacitorless 1T-DRAM: From Single-Gate PD-SOI to Double-Gate FinDRAM", 2004 IEEE International Electron Devices Meeting Technical Digest, December 2004, 4 pages.			L
		T. M. MAYER, et al., "Chemical Vapor Deposition of Fluoroalkylsilane Monolayer Films for Adhesion Control in Microelectromechanical Systems" 2000 American Vacuum Society B 18(5), Sep/Oct 2000, pp. 2433-2440			
Examiner Signature				Date Considered	

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